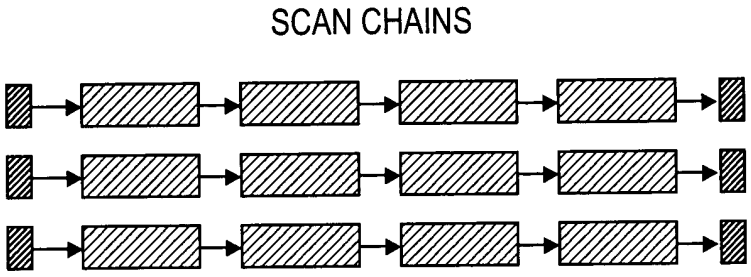
SCAN CHAINS

FIG. 1

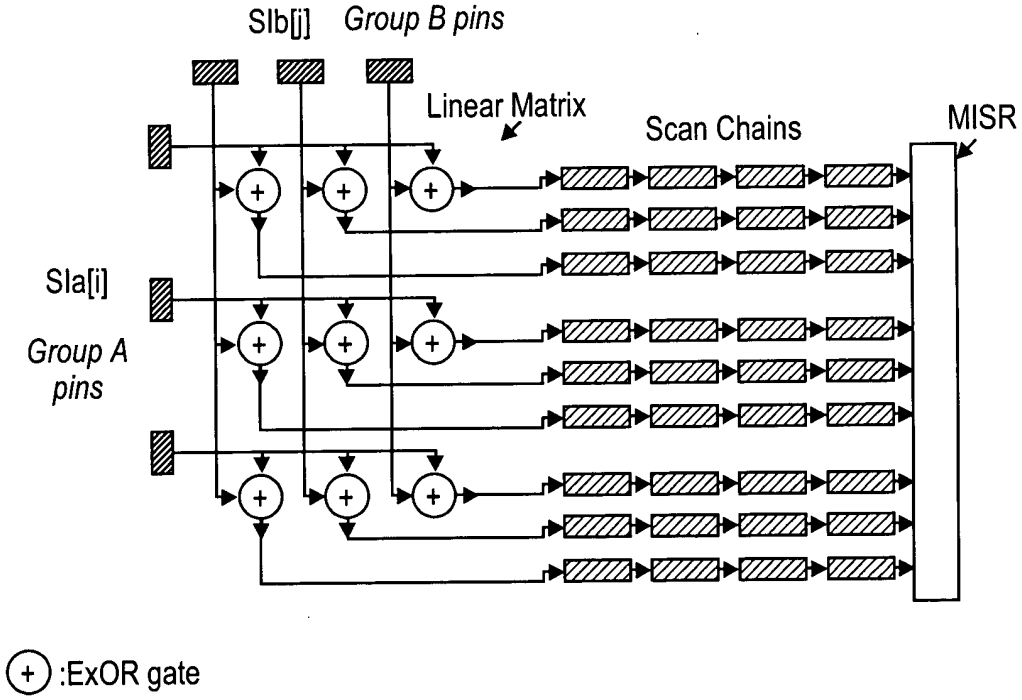
SIb[j]
Group B pins
Linear Matrix
Scan Chains
MISR
SIa[i]
Group A pins
+ :ExOR gate

FIG. 2

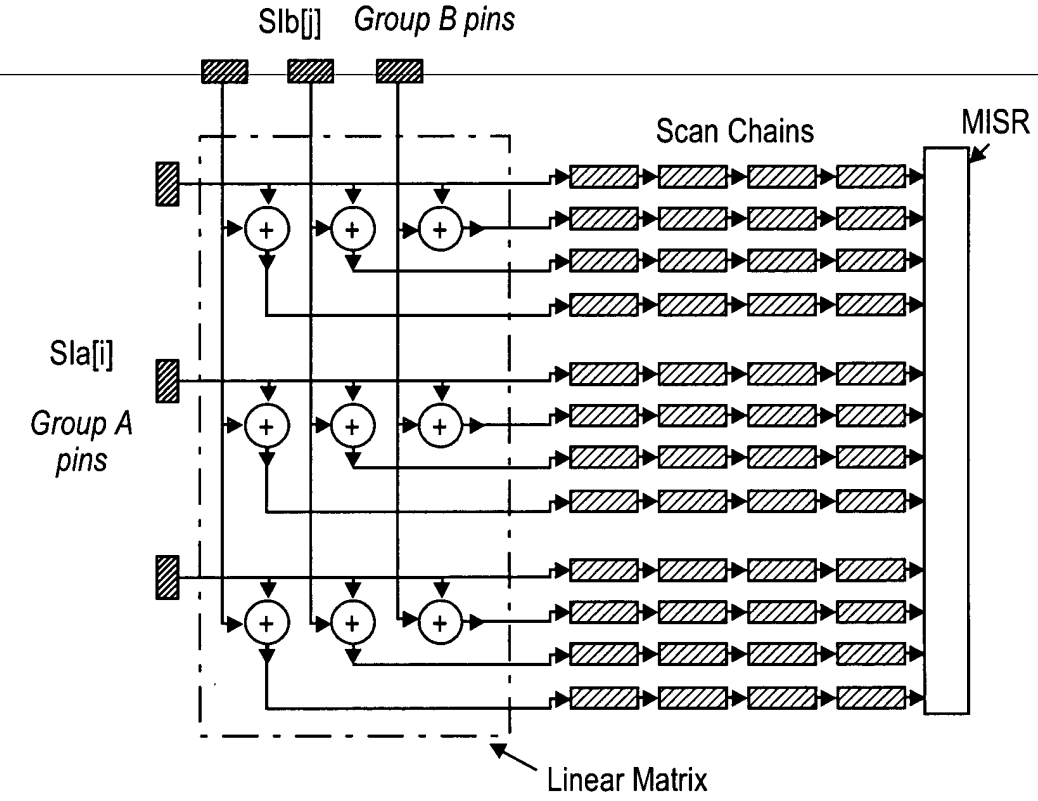
SIb[j]
Group B pins
Scan Chains
MISR
SIa[i]
Group A pins
Linear Matrix
+ :ExOR gate

FIG. 3

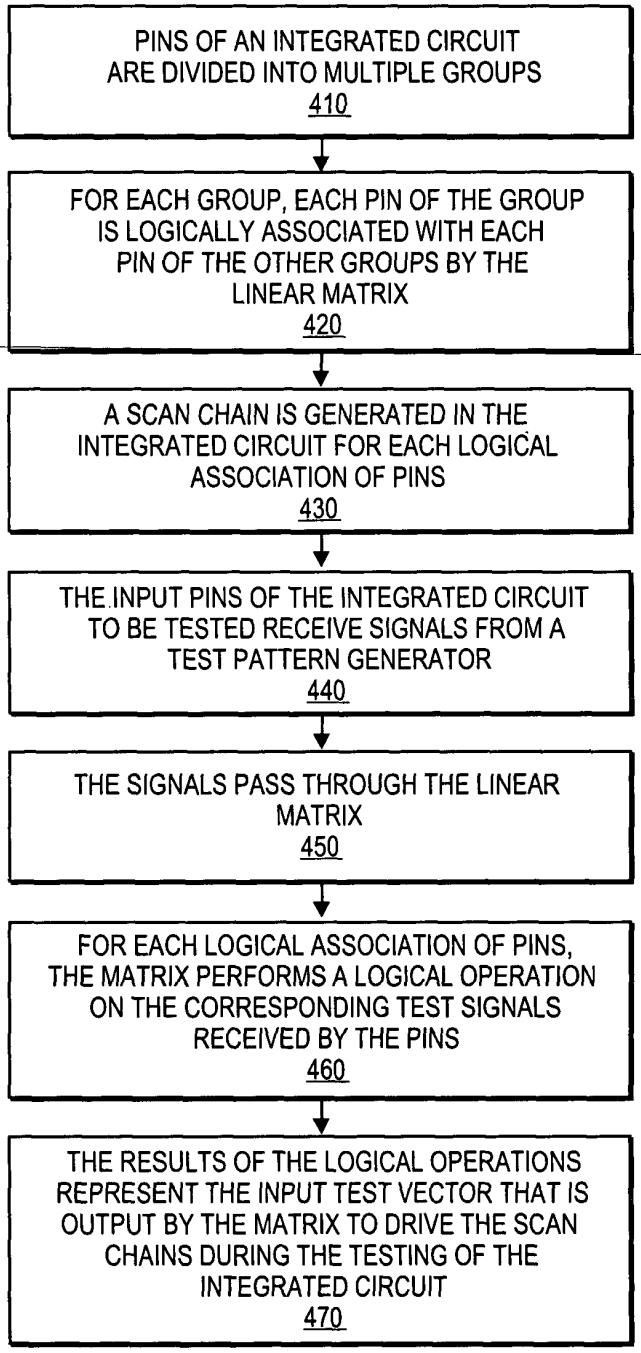
PINS OF AN INTEGRATED CIRCUIT ARE DIVIDED INTO MULTIPLE GROUPS
410
FOR EACH GROUP, EACH PIN OF THE GROUP IS LOGICALLY ASSOCIATED WITH EACH PIN OF THE OTHER GROUPS BY THE LINEAR MATRIX
420
A SCAN CHAIN IS GENERATED IN THE INTEGRATED CIRCUIT FOR EACH LOGICAL ASSOCIATION OF PINS
430
THE INPUT PINS OF THE INTEGRATED CIRCUIT TO BE TESTED RECEIVE SIGNALS FROM A TEST PATTERN GENERATOR
440
THE SIGNALS PASS THROUGH THE LINEAR MATRIX
450
FOR EACH LOGICAL ASSOCIATION OF PINS, THE MATRIX PERFORMS A LOGICAL OPERATION ON THE CORRESPONDING TEST SIGNALS RECEIVED BY THE PINS
460
THE RESULTS OF THE LOGICAL OPERATIONS REPRESENT THE INPUT TEST VECTOR THAT IS OUTPUT BY THE MATRIX TO DRIVE THE SCAN CHAINS DURING THE TESTING OF THE INTEGRATED CIRCUIT
470

FIG. 4